CLAIMS

1.   A method comprising:

generating a system object including a plurality of nodes and channels; and

generating a data structure describing said system object, said data structure describing said plurality of nodes, each of said nodes comprising an adaptive computing device.

2.   The method of claim 1, wherein each of said nodes comprises an FPGA (Field Programmable Gate Array)-based adaptive computing device.

3.   The method of claim 1, further comprising interconnecting first-in first out (FIFO) registers associated with said adaptive computing devices to create channels between said devices.

4.   The method of claim 1, further comprising destroying the system object.

5.   The method of claim 1, wherein said generating the system object comprises generating a ring system object comprising a ring of nodes.

6. The method of claim 1, further comprising configuring at least one of said plurality of nodes.

7. The method of claim 6, wherein said configuring comprises:

generating a configuration data structure; and

sending a bitstream to said node as specified in a configuration data structure.

8. The method of claim 7, wherein said configuration data structure includes information identifying nodes to configure.

9. The method of claim 7, wherein said configuration data structure includes device-level configuration information for configuring an adaptive computing device.

10. The method of claim 1, wherein said generating a system object comprises executing instructions defining said system object on a first platform.

11. The method of claim 10, further comprising:

executing said instructions defining said system on a second platform; and

generating said system object on a second platform in response to said executing the instructions.

12. The apparatus of claim 11, wherein the first platform comprises a cluster of workstations, each workstation including a processor connected to an adaptive computing device.

13. The apparatus of claim 12, wherein the adaptive computing devices are connected to a PCI (Peripheral Component Interconnect) bus.

14. The apparatus of claim 12, wherein the second platform comprises an embedded system including a host processor connected to a plurality of adaptive computing devices.

15. The apparatus of claim 14, wherein the plurality of adaptive computing devices are connected to a VME (Versa Module Europa) bus.

16. An article comprising a machine-readable medium including machine-executable instructions, the instructions operative to cause a machine to:

generate a system object including a plurality of nodes and channels; and

generate a data structure describing said system object, said data structure describing said plurality of nodes, each of said nodes comprising an adaptive computing device.

17. The article of claim 16, wherein each of said nodes comprises an FPGA (Field Programmable Gate Array)-based adaptive computing device.

18. The article of claim 16, further comprising instructions operative to cause the machine to interconnect first-in first out (FIFO) registers associated with said adaptive computing devices to create channels between said devices.

19. The article of claim 16, further comprising instructions operative to cause the machine to destroy the system object.

20. The article of claim 16, wherein the instructions for generating the system object comprise instructions operative to cause the machine to generate a ring system object comprising a ring of nodes.

21. The article of claim 16, further comprising instructions operative to cause the machine to configure at least one of said plurality of nodes.

22. The article of claim 21, wherein the instructions for configuring comprise instructions operative to cause the machine to:

generate a configuration data structure; and

send a bitstream to said node as specified in a configuration data structure.

23. The article of claim 22, wherein said configuration data structure includes information identifying nodes to configure.

24. The article of claim 22, wherein said configuration data structure includes device-level

configuration information for configuring an adaptive computing device.

25.   The article of claim 16, wherein the instructions for generating a system object comprise instructions operative to cause a machine on a first platform to define said system object and to cause a machine on a second platform to define said system object.

26.   The article of claim 25, wherein the first platform comprises a cluster of workstations, each workstation including a processor connected to an adaptive computing device.

27.   The article of claim 26, wherein the adaptive computing devices are connected to a PCI (Peripheral Component Interconnect) bus.

28.   The article of claim 27, wherein the second platform comprises an embedded system including a host processor connected to a plurality of adaptive computing devices.

29. The article of claim 28, wherein the plurality of adaptive computing devices are connected to a VME (Versa Module Europa) bus.

30. Apparatus comprising:

a plurality of adaptive computing elements connected in a ring configuration, including

a plurality of processing elements connected in a chain configuration and including a first processing element at a first end of the chain and a second processing element at a second end of the chain, and

a control element connected to the first processing element and the second processing element, and operative to manage data entering the ring;

a bus; and

an interface device connected between the control element and the bus.

31. The apparatus of claim 30, wherein each of the adaptive computing elements comprises an FPGA (Field Programmable Gate Array) integrated circuit.

32. The apparatus of claim 30, wherein the ring includes two processing elements.

33. The apparatus of claim 32, further comprising a cross-bar data path connecting the control element to each of the two processing elements.

34. The apparatus of claim 30, wherein the bus comprises a PCI (Peripheral Component Interconnect) bus.

35. The apparatus of claim 30, wherein the bus comprises a VME (Versa Module Europa) bus.

36. The apparatus of claim 30, further comprising a host processor connected to the bus and operative to configure the adaptive computing elements.

37. The apparatus of claim 30, wherein the apparatus comprises an adaptive computing system (ACS) accelerator.

38.   The apparatus of claim 30, further comprising a memory device connected to each of the processing elements.

39.   The apparatus of claim 38, wherein each memory device comprises an SRAM (Static Random Access Memory).

40.   The apparatus of claim 30, wherein the interface device is integrated in the control element.

41.   The apparatus of claim 30, further comprising an integrated circuit including the processing elements and the control element.

42.   The apparatus of claim 30, wherein the interfaces device comprises an FPGA (Field Programmable Gate Array) integrated circuit.

43.   The apparatus of claim 30, further comprising:

a second plurality of adaptive computing elements connected in a second ring configuration, including

a plurality of processing elements connected in a chain configuration and including a third processing element at a first end of the chain and a fourth processing element at a second end of the chain, and

a control element connected to the first processing element and the second processing element, and operative to manage data entering the ring;

a first data path connected the first processing element and the fourth processing element; and

a second data path connected between the second processing element and the third processing element.